REMARKS

Claims 1-22, 25 and 31-46 were pending in the parent application hereto, U.S. Serial No. 09/801,241. Applicant has filed herewith a Request for Continued Examination (RCE) to further prosecute this application. By this paper, Applicant has cancelled Claims 18-22 and 25 without prejudice, and amended Claims 1, 7, 9, 31, 37-44 and 46. Accordingly, Claims 1-17 and 31-46 are presented herein for examination.

*Advisory Action and Non-entry of Amendments*

Per the Advisory Action, Applicant's amendments filed with its Amendment and Response to Final Office Action dated December 6, 2004 were not entered by the Examiner. Accordingly, Applicant herein again provides these amendments and remarks pursuant to the above-referenced RCE.

*Claim Identifiers*

Per Par. 1 of the Final Office Action, Applicant has herein corrected all claim identifiers as requested. Applicant submits that these amendments overcome the Examiner's objections.

*Specification*

Per Par. 2 of the Final Office Action Applicant has amended the specification to define the first occurrence of the term "HDL". Applicant submits that these amendments overcome the Examiner's objections.

*Claim Objections*

Per Par. 3, page 2 of the Final Office Action, Claim 37 and various other claims cited by the Examiner have been amended herein to correct the cited informalities. Applicant submits that these amendments overcome the Examiner's objections.

*§112 Rejections*

Per Pars. 4-10 of the Final Office Action, Claim 31 and various other claims cited by the Examiner have been amended herein to overcome the Examiner's rejections.

*§102 Rejections*

By this paper, Applicant has cancelled all Claims rejected under 35 U.S.C. § 102, thereby rendering all such rejections moot.

*§103 Rejections*

By this paper, Applicant has amended independent Claims 1, 9, 31, 37, 40, 41, 42, 43, 44 and 46 to include limitations which Applicant respectively submits are in no way taught or suggested by the art of record when considered in combination with the other recited limitations of these claims.

Specifically, Studor is representative of a class of art Applicant refers to as "*ex post facto*" extensibility; i.e., where the design of the core (e.g., CPU) is determined and solidified well before the extension hardware and/or instructions are added to the device. See, e.g., Col. 2, lines 48-56 of Studor:

> *"A simple and cost effective way to add new instructions to a central processing unit (CPU) was needed. By modifying the architecture of a new or prior art CPU, the new or prior art CPU can be made extensible so that new instructions cane {sic} be added in a relatively simple and cost effective manner. The term "extensible" in regard to a CPU is used to mean that new instructions can be added to the CPU simply by adding certain designated circuitry,* ***without the need to significantly change the existing CPU circuitry****."*

See also Col. 3, lines 10-18:

> *"A prior art CPU can be made extensible by making the following modifications: (1) allowing more than one control unit to drive the control signals into the execution unit; (2) locating all of the registers in the programmer's model in the execution unit (including the condition code register); (3) modifying the state sequencer circuitry; and (4) adding a few control signals. Once the CPU is extensible, additional instructions can be added* ***without any significant changes to the extensible CPU circuitry****."*

Hence, the entire focus of Studor is to modify an existing (or new) CPU configuration with features that allow extensions to be subsequently added to the core without requiring any (significant) changes to the core. Stated differently, Studor takes a core (such as the Motorola MC68HC05 family microcontroller described therein) and adds components that allow the subsequent addition of extension instructions, thereby obviating any further modifications to the core.

See also U.S. Patent No. 4,763,242 to Lee, et al, which is generally cumulative to Studor but illustrates this class of art as well.

Contrast the foregoing approaches with that of Applicant's invention, wherein one or more selections made by the user at the time of design of the core are at least in part determinative of the core configuration. For example, the user may select a given core architecture, bus architecture, cache configuration, etc., as well as adding one or more extensions, and the description of the device as a whole subsequently generated as a cohesive design. Specifically, Applicant's approach significantly reduces gate count and power consumption over prior art approaches such as those of Studor, since the core is in effect substantially redesigned around the selected architecture, cache configuration, extension(s), etc. The Examiner is respectfully referenced to Applicant's co-pending U.S. patent application Serial No. 09/418,663 entitled "Method and Apparatus for Managing the Configuration and Functionality of a Semiconductor Design" filed October 14, 1999, which was incorporated in the instant application by reference in its entirety at time of filing. This disclosure describes in detail an exemplary configuration of Applicant's design environment which incorporates the foregoing advantages.

As to Claims 41 and 43, Applicant's approach also renders other benefits relating to integration of macrofunctions (such as DSP and I/O): See, e.g., Applicant's specification as filed, which states:

> "*The extensible nature of certain processor cores (e.g., the Applicant's "ARC" core) and associated XY memory allow DSP and I/O functions to be tightly coupled for such demanding applications.*" [Page 8, lines 28-30]; and

> *"It is noted that different DSP cores (or other types of processor cores) will generally have varying interface, control and memory requirements. The interface 200 of the present invention advantageously provides the designer with the ability to integrate cores of various configurations directly with the parent processor core (e.g., extensible ARC processor) instruction and operand decode mechanism, auxiliary register, and on-core memory resources."* [Page 12, lines 1-6].

Hence, whereas the approach of Studor or Lee would be to add the macrofunction (e.g., DSP or I/O) to a substantially stagnant or predefined core, Applicant's approach utilizes inputs received from the designer regarding both the core configuration and the macrofunctions, and produces a resultant design wherein the core and macrofunction configurations are tightly coupled. Applicant respectfully submits that neither Blackmon (U.S. 6,628,662), Goodwin (U.S. 6,125429) nor Studor teach or suggest such functionality. Hence, as a matter of law, the combination of these references cannot render Applicant's claimed inventions as presented herein obvious.

Applicant further submits that in addition to not teaching or fairly suggesting all of the limitations of Applicant's claims as amended herein, Studor teaches away from Blackman or Goodwin to produce Applicant's invention(s). As previously noted, Studor teaches an *ex post facto* approach to processor extension which pointedly seeks to minimize the changes to the core (*"Once the CPU is extensible, additional instructions can be added without any significant changes to the extensible CPU circuitry."*). Hence, one would not fairly be led to combine Studor with Blackman, Goodwin, or other such art to produce Applicant's claimed inventions, since Applicant's claimed inventions purposely seek to modify at least portions of the core in order to more "tightly couple" the extension hardware and/or macrofunctions to the core as previously described. This again underscores the salient distinction between such *ex post facto* extensibility and that of Applicant's invention.

As to Claim 42, Applicant has amended this claim to include limitations relating to a prototype core template, such approach being described in the aforementioned Application Serial No. 09/418,663. None of the aforementioned references relied on by the Examiner teach or suggest such functionality.

*Summary*

Based on Applicant's cancellation herein of all claims rejected under §102, and amendment of all remaining independent claims rejected under §103, Applicant respectfully submits that all pending claims distinguish over the art of record, and are in condition for allowance.

*Other Remarks*

Applicant hereby specifically reserves the right to prosecute claims of different or broader scope in a continuation or divisional application.

Applicant notes that any claim cancellations or additions made herein are made solely for the purposes of more clearly and particularly describing and claiming the invention and responding to the aforementioned restriction election, and not for purposes of overcoming art or for patentability. The Examiner should infer no (i) adoption of a position with respect to patentability, (ii) change in the Applicant's position with respect to any claim or subject matter of the invention, or (iii) acquiescence in any way to any position taken by the Examiner, based on such cancellations or additions.

Furthermore, any remarks made with respect to a given claim or claims are limited solely to such claim or claims.

If the Examiner has any questions or comments that may be resolved over the telephone, he/she is requested to call the undersigned at (858) 675-1670.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

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